Amendments to the Specification

Please amend the second whole paragraph on Page 7 of the application as follows.

Referring to FIG. 2, FIG. 3A, [[and]] FIG. 3B, and FIG. 5C a p-type semiconductor substrate (P-sub for short in figures) 100 is provided and can be divided into a memory area I and a peripheral circuit area II. An isolation region 102, such as a field oxide layer or shallow trench isolation, is formed in the substrate 100 to define striped active areas AA. The striped active areas AA are parallel to each other.